REMARKS/ARGUMENTS

Applicants have amended Claims 8-9, and added new Claims 24-29. Applicants submit that no new matter has been added.

Applicants have cancelled Claims 1 – 7, 16 and 19-23.

Claims 8-15, 17-18, and 24-29 are now in the present application for examination.

Applicants respectfully request reconsideration in light of the following remarks.

Claim Rejections – 35 USC § 112

Claim 16 is rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. There is insufficient antecedent basis for this limitation "the second dielectric layer" in Claim 16.

Applicants have cancelled Claim 16, thus withdrawal of the claim rejection under 35 U.S.C. Section 112 is respectfully requested.

Claim Rejections – 35 USC § 103

Claims 8-18 are rejected under 35 U.S.C.103(a) as being unpatentable over Sheu et al. (US 6,146,950) in view of Okada et al. (US 6,383,910).

Applicants respectfully traverse the rejection made by the Examiner for the reasons discussed below.

The claimed invention provides a method of manufacturing a mask read only memory, which comprises sequential steps of providing a semiconductor structure having a first opening therein, forming a first glue layer on a surface of the semiconductor structure extending into the first opening, forming a contact

plug within the first opening in the semiconductor structure, the contact plug comprising a first glue layer lining the first opening and a first metal layer in the first opening, etching the first glue layer outside the contact plug in order to expose the surface of the semiconductor structure, forming a patterned photoresist layer on the semiconductor structure, and forming a plurality of code areas in the semiconductor structure by using the patterned photoresist layer as a mask.

A key feature of the claimed invention is "to etch the first glue layer outside the contact plug to expose the surface of the semiconductor structure first, and then form the patterned photoresist layer as a mask for forming the plurality of code areas in the semiconductor structure", which has been recited in the amended independent Claim 8. Since the first glue layer outside the contact plug is removed first, then the patterned photoresist layer can be directly used as the mask to form the plurality of code areas in the semiconductor structure, i.e. the first glue layer is not necessary to be removed after the patterned photoresist layer is formed as the mask for forming the code areas. Thus, the implanted profile of the code areas formed by an ion implantation process can be effectively improved, and the critical dimension of the code areas can be simply defined by the resolution limit of lithography.

In the cited patent '950, Sheu et al. provide a method of manufacturing multiple metallic layered embedded read-only-memory (ROM), which comprises providing a substrate having a memory cell region and a peripheral circuit region thereon, forming a first dielectric layer over the substrate, forming a first contact in the first dielectric layer in the periphery circuit region, forming a first patterned metallic layer that couple electrically with the first contact in the

peripheral circuit region, forming a second dielectric layer over the substrate, removing a portion of the second dielectric layer in the memory cell region to form a remaining second dielectric layer having a sloping sidewall surrounds a periphery of the memory cell region, forming a via hole in the second dielectric layer in the peripheral circuit region and a second contact opening in the first dielectric layer in the memory cell region, wherein the via hole exposes the first patterned metallic layer, forming a metallic barrier layer over the substrate, coding by implanting ions into coded regions in the substrate, forming a second patterned metallic layer in the peripheral circuit region to cover the second dielectric layer and fill the via hole to electrically coupled with the first patterned metallic layer, forming a third patterned metallic layer in the memory cell region to fill the contact opening, and forming a passivation layer over the substrate.

In the cited patent '910, Okada et al. provide a method of manufacturing a semiconductor device, which comprises a step of forming a second glue layer on a semiconductor structure.

Regarding the amended Claim 8, there is no teaching in the cited patent '950 "to etch the first glue layer outside the contact plug to expose the surface of the semiconductor structure first, and then to form the patterned photoresist layer as a mask for forming the plurality of code areas in the semiconductor structure". See column 5, lines 50-53, and column 6, lines 13-26 of the cited patent '950, the metallic barrier layer 234 (i.e. the first glue layer of the claimed invention) is removed after forming the coding mask layer 236. Accordingly, Applicants respectfully submit that the cited references, either alone or in combination, fail to disclose or render obvious the feature of the claimed

invention as set forth in the amended independent Claim 8.

Regarding Claim 12, Examiner states that Okada teaches planarizing the first metal layer to form the contact plug (see Okada at column 9, lines 47-50), and regarding Claim 14, Examiner states that Okada teaches etching the first glue layer outside the contact plug in order to expose the surface of the semiconductor structure comprising a blanket etching back process (see Okada at column 6, lines 15-19). However, see column 3, lines 13-20, and column 6, lines 27-32 of the cited patent '950, since the dielectric layer sloping sidewall 230 is formed to prevent short-circuiting between the neighboring conductive lines, one of ordinary skill in the art would not planarize the first metal layer to form the contact plug or etch the first glue layer outside the contact plug by a blanket etching back process as suggested by Okada in the presence of the sloping sidewall 230.

It is therefore Applicants' belief that Claim 8 is allowable over the cited references. Insofar as Claims 9-15, 17-18, and 24-29 depend from Claim 8, it is Applicants' belief that these Claims are also considered to be allowable. Reconsideration and withdrawal of the rejection under 35 U.S.C. Section 103 are respectfully requested.

Conclusion

In the light of the above remarks, Applicants respectfully submit that pending Claims 8-15, 17-18, and 24-29 as currently presented are in condition for allowance. Reconsideration is respectfully requested.

Respectfully submitted,
Liu ET AL

Dated: 02/13/2007

Squire, Sanders & Dempsey L.L.P.
600 Hansen Way
Palo Alto, CA 94304-1043
Telephone (650) 843-3375
Facsimile (650) 843-8777

By /Aaron Wininger, Reg. No. 45,229/
Aaron Wininger
Attorney for Applicants
Reg. No. 45,229